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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,310	01/22/2004	Yasunaga Iseda	61282-057	3085

7590 01/26/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,310	ISEDA ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- Th MAILING DATE of this communication appears on th cover sh t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *6-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,9,10,12,13,15 and 16* is/are rejected.

7)☒ Claim(s) *2,5,11,14 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 01/22/2004 is acceptable.

Election/ Restriction

2. Applicant's election of **Invention I, claims 1-5 and 9-17** in the reply filed on 01/06/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

3. **Claims 6-8** withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore:

The "connected to a different node" in "said bump is formed outside above the edge of the uppermost layer wiring connected to a different node from that of the rewiring layer connected to said bump" of **claim 3** and in "arranging said bump so that it is located outside above the edge of said uppermost layer wiring connected to a different node from that of the

rewiring layer connected to said bump" of **claim 9** must be shown or the feature(s) canceled from the claim(s);

The "connected to the same node" in "wherein said bump is formed outside above the edge of said uppermost layer wiring connected to the same node as that of the rewiring layer connected to said bump" and in "said bump is formed outside above the edge of the uppermost layer wiring connected to a different node from that of the rewiring layer connected to said bump" of **claim 4** and the limitation "connected to the same node" in "said uppermost layer wiring connected to the same node as that of the rewiring layer connected to said bump" and in "arranging said bump so that it is located outside above the edge of said uppermost layer wiring connected to a different node from that of the rewiring layer connected to said bump" of **claim 10** must be shown or the feature(s) canceled from the claim(s); and

The "outside a region where said uppermost layer wiring exists" in "arranging said bump so that it is located outside a region where said uppermost layer wiring exists" of **claim 12** must be shown or the feature(s) canceled from the claim(s).

No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

5. **Claims 13-17** are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of these claims recites: a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim xx is located beneath each of all bumps, where xx is the respective claim from which each of these claims depend. It is not clear which element is "located beneath each of all bumps". For examination purpose, the uppermost layer element wiring structure is located beneath each of all bumps, and each of these claims should be rewritten as:

A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim xx such that the uppermost layer element wiring structure is located beneath each of all bumps.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 3, 9, 13, and 15** are rejected under 35 U.S.C. §103(a) as being unpatentable over Nishimoto et al. U.S. Patent 6,812,565 (the '565 patent).

The '565 patent discloses in Figs. 15 and 16 and respective portions of the specification a semiconductor device and a method of designing thereof substantially as claimed.

Referring to **claim 1**, the '565 patent discloses a semiconductor device comprising:

an uppermost layer wiring (14, column 8, lines 19-40) formed on a semiconductor substrate (2, which is a "memory chip", and "substrate" is interpreted broadly);

a rewiring layer (9/9A) formed so as to be connected to said uppermost layer wiring; and

a bump (4) connected to said rewiring layer, wherein said semiconductor device has at least one uppermost layer element wiring structure located below said bump and having the uppermost layer wiring with a larger area (as is evident from Fig. 16, and where "area" is interpreted broadly) than a connecting area between said bump and said rewiring layer.

Referring to independent **claim 3** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the '565 patent discloses a semiconductor device comprising:

an uppermost layer wiring formed on a semiconductor substrate;

a rewiring layer (9/9A, 9 not visible in Fig. 16) formed so as to be connected ("connected" is interpreted broadly) to said uppermost layer wiring; and a bump connected to said rewiring layer,

wherein said bump (right bump 4, Fig. 16) is formed outside above the edge of the uppermost layer wiring (14) connected to a different node from that of the rewiring layer connected to said bump.

Referring to independent **claim 9** and using the same reference characters, citations, and interpretations as detailed above for claim 1 and/or claim 3 where applicable, the '565 patent discloses a method of designing a semiconductor device comprising an uppermost layer wiring formed on a semiconductor substrate, a rewiring layer formed and a bump connected to said rewiring layer, wherein a process of arranging said bump comprises a step of:

arranging said bump so that it is located outside above the edge of said uppermost layer wiring connected to a different node from that of the rewiring layer (9/9A, 9 not visible in Fig. 16) connected to said bump.

However, for each of claims 1, 3, and 9 thus disclosed, the '565 patent teaches, instead of a protection film as claimed, a plurality of protection film (13/15) through which said rewiring layer formed so as to be connected to said uppermost layer wiring.

Nevertheless, since the disclosed multi-layered film 13/15 is functionally equivalent to the claimed single layer protection film, and since both the reference and the present invention have failed to articulate as to why the multi-layered protection film would not function as the single-layer protection film, the change from one to the other would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claims 13 and 15**, although the '565 patent fails to disclose a step of arranging the uppermost layer element wiring structure described in claim 1 and 3 such that the uppermost layer element wiring structure is located beneath each of all bumps, from Figs. 15 and 16, the uppermost layer element wiring structure described above for claim 1 and 3 appears to be located beneath each of all bumps, which "beneath" and "connected" both interpreted as broadly as the claims.

7. **Claims 1, 3, 9, 12-13, and 15** are rejected under 35 U.S.C. §103(a) as being unpatentable over Figs. 7's of Aoki et al. U.S. Patent 6,545,354 (the '354 patent).

The '354 patent discloses in Figs. 7's and respective portions of the specification a semiconductor device and a method of designing thereof substantially as claimed.

Referring to **claim 1**, the '354 patent discloses a semiconductor device comprising:

an uppermost layer wiring (3/3a of Fig. 7A, "wiring segment", column 1, lines 30-67, and as it is formed on the uppermost surface of the semiconductor substrate 1, it is an uppermost layer wiring) formed on a semiconductor substrate (1);

a rewiring layer (7/7a, "re-wiring segment") formed so as to be connected to said uppermost layer wiring; and

a bump (not shown, column 1, lines 59-61) connected to said rewiring layer, wherein said semiconductor device has at least one uppermost layer element wiring structure located below said bump and having the uppermost layer wiring with a larger area (as is evident from Fig. 7A, and where "area" is interpreted broadly) than a connecting area between said bump and said rewiring layer.

Referring to independent **claim 3** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the '354 patent discloses a semiconductor device comprising:

an uppermost layer wiring (left wiring layer 3/3a) formed on a semiconductor substrate;

a rewiring layer (right rewiring layer 7/7a) formed so as to be connected ("connected" is interpreted as broadly as the claim) to said uppermost layer wiring; and a bump (not showed) connected to said rewiring layer,

wherein said bump (right not-shown bump, which is to be directly connected to and in direct contact with right element 8 as is known in the art) is formed outside above the edge of the uppermost layer wiring (left wiring layer 3/3a) connected to a different node from that of the rewiring layer connected to said bump.

Referring to independent **claim 9** and using the same reference characters, citations, and interpretations as detailed above for claim 1 and/or claim 3 where applicable, the '354 patent discloses a method of designing a semiconductor device comprising an uppermost layer wiring formed on a semiconductor substrate, a rewiring layer formed and a bump connected to said rewiring layer, wherein a process of arranging said bump comprises a step of:

arranging said bump so that it is located outside above the edge of said uppermost layer wiring connected to a different node from that of the rewiring layer connected to said bump.

However, for each of claims 1, 3, and 9 thus disclosed, the '354 patent teaches, instead of a protection film as claimed, a plurality of protection film (4/5) through which said rewiring layer formed so as to be connected to said uppermost layer wiring.

Nevertheless, since the disclosed multi-layered film 4/5 is functionally equivalent to the claimed single layer protection film, and since both the reference and the present invention have failed to articulate as to why the multi-layered protection film would not function as the single-layer protection film, the change from one to the other would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claims 13 and 15**, although the '354 patent fails to disclose a step of arranging the uppermost layer element wiring structure described in claim 1 and 3 such that the uppermost layer element wiring structure is located beneath each of all bumps, from Figs. 7's, the uppermost layer element wiring structure described above for claim 1 and 3 appears to be located beneath each of all bumps, which "beneath" and "connected" both interpreted as broadly as the claims.

Referring to **claim 12**, the '354 patent further discloses that the process of arranging said (not-shown, on-the-right) bump comprises a step of: arranging said bump so that it is located outside a region where said (left) uppermost layer wiring exists.

8. **Claims 1, 3-4, 9-10, 13, 15, and 16** are rejected under 35 U.S.C. §103(a) as being unpatentable over Figs. 2A of the '354 patent.

The '354 patent discloses in Fig. 2A and respective portions of the specification a semiconductor device and a method of designing thereof substantially as claimed.

Referring to **claim 1**, the '354 patent discloses a semiconductor device comprising:

an uppermost layer wiring (13/13a, "wiring segment", column 4, lines 19-67, and as it is formed on the uppermost surface of the semiconductor substrate 11, it is an uppermost layer wiring) formed on a semiconductor substrate (11);

a rewiring layer (31/31a/31b, "inductor", column 5, lines 19-67, and note that although for this embodiment it is called "inductor", the functional equivalents in the other embodiments and of the prior art are called rewiring segment, as detailed above) formed so as to be connected to said uppermost layer wiring; and

a bump (not shown, column 1, lines 59-61, and note that although this passage is disclosed specifically for prior art Fig. 7, it is also for Fig. 2A because Fig. 2A appears to be an improvement over Fig. 7 or because no bump-less connection is disclosed) connected to said rewiring layer, wherein said semiconductor device has at least one uppermost layer element wiring structure located below said bump and having the uppermost layer wiring with a larger area (as is evident from Fig. 2A, and where "area" is interpreted broadly) than a connecting area between said bump and said rewiring layer.

Referring to independent **claim 3** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the '354 patent discloses a semiconductor device comprising:

an uppermost layer wiring (comprising both left and right portions of uppermost wiring layer 13/13a) formed on a semiconductor substrate;

a rewiring layer (31/31a/31b) formed so as to be connected ("connected" is interpreted as broadly as the claim) to said uppermost layer wiring; and a bump (not showed, the center of the

three not-shown bumps connected to the respective elements 21) connected to said rewiring layer,

wherein said bump is formed outside above the edge of the uppermost layer wiring (the left portion) connected to a different node from that of the rewiring layer connected to said bump.

Referring to independent **claim 9** and using the same reference characters, citations, and interpretations as detailed above for claim 1 and/or claim 3 where applicable, the '354 patent discloses a method of designing a semiconductor device comprising an uppermost layer wiring formed on a semiconductor substrate, a rewiring layer formed and a bump connected to said rewiring layer, wherein a process of arranging said bump comprises a step of:

arranging said (center not-shown) bump so that it is located outside above the edge of said uppermost layer wiring connected to a different node from that of the rewiring layer connected to said bump.

However, for each of claims 1, 3, and 9 thus disclosed, the '354 patent teaches, instead of a protection film as claimed, a plurality of protection film (14/16/18) through which said rewiring layer formed so as to be connected to said uppermost layer wiring.

Nevertheless, since the disclosed multi-layered film 14/16/18 is functionally equivalent to the claimed single layer protection film, and since both the reference and the present invention have failed to articulate as to why the multi-layered protection film would not function as the single-layer protection film, the change from one to the other would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claims 13 and 15**, although the '354 patent fails to disclose a step of arranging the uppermost layer element wiring structure described in claim 1 and 3 such that the uppermost layer element wiring structure is located beneath each of all bumps, from Figs. 2A and 2B, the uppermost layer element wiring structure described above for claim 1 and 3 appears to be located beneath each of all bumps, which "beneath" and "connected" both interpreted as broadly as the claims.

Referring to **claim 4**, the '354 patent further discloses that said (center not-shown) bump is formed outside above the edge of (the right portion of) said uppermost layer wiring connected to the same node as that of the rewiring layer connected to said bump.

Referring to **claim 10**, the '354 patent further discloses arranging said (center not-shown) bump so that it is located outside above the edge of (the right portion of) said uppermost layer wiring connected to the same node as that of the rewiring layer connected to said bump.

Referring to **claim 16**, although the '354 patent fails to disclose a step of arranging the uppermost layer element wiring structure described in claim 4 such that the uppermost layer element wiring structure is located beneath each of all bumps, from Figs. 2A and 2B, the uppermost layer element wiring structure described above for claim 4 appears to be located beneath each of all bumps, which "beneath" and "connected" both interpreted as broadly as the claims.

Allowable Subject Matter

9. **Claims 2, 5, and 11**, and dependent **claims 14 and 17**, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device and a method of designing thereof having all exclusive limitations as recited in claims 1/2 (claims 1 and 2), 3/5, and 9/11, characterize in that said bump is formed within a region of a wiring width of said uppermost layer wiring.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
January 21, 2005

David Nelms
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